

CLAIMS

We claim:

1 1. An interconnect structure comprising:
2 a substrate;
3 a plated through hole positioned within the substrate;
4 a redistribution layer on a first and a second surface of
5 the substrate; and
6 a via within the redistribution layer, selectively
7 positioned ~~over~~^{ed to} and electrically connecting the plated through
8 hole. *In line w/*

1 2. The interconnect structure of claim 1, wherein the substrate
2 comprises:

3 a ground plane;
4 a first dielectric layer over a first and a second side of
5 the ground plane;
6 a first pair of first signal planes, one over each first
7 dielectric layer;
8 a second dielectric layer substantially over each first
9 signal plane;
10 a first pair of first power planes, one over each second
11 dielectric layer;
12 a third dielectric layer substantially over each first power
13 plane;

14 a second pair of second signal planes, one over each third
15 dielectric layer;
16 a fourth dielectric layer substantially over each second
17 signal plane; and
18 a second pair of second power planes, one over each fourth
19 dielectric layer.

1 3. The interconnect structure of claim 2, wherein the ground
2 plane comprises copper-Invar-copper.

1 4. The interconnect structure of claim 2, wherein the first and
2 second signal planes are layers of controlled impedance
3 circuitry.

1 5. The interconnect structure of claim 2, wherein the first,
2 second, third and fourth dielectric layers comprise a
3 polytetrafluoroethylene material filled with silicon particles.

1 6. The interconnect structure of claim 1, wherein the
2 redistribution layer comprises a fatigue resistant dielectric
3 material.

1 7. The interconnect structure of claim 1, wherein the via
2 includes a portion of a chip connector.

1 8. The interconnect structure of claim 7, wherein the chip
2 connector is selected from the group consisting of: controlled
3 collapse chip connectors, ball grid array connectors and reflow
4 solder attach connectors.

1 9. The interconnect structure of claim 1, wherein the via is
2 offset from the center of the plated through hole.

1 10. The interconnect structure of claim 1, wherein the plated
2 through hole includes copper plating.

1 11. The interconnect structure of claim 1, wherein the plated
2 through hole further includes a fill material.

1 12. The interconnect structure of claim 11, wherein the fill
2 material is a reinforcing material.

1 13. The interconnect structure of claim 12, wherein the
2 reinforcing material comprises an electrically conductive
3 material.

1 14. The interconnection structure of claim 1, further including a
2 buried plated through hole within the substrate.

3 15. A method of forming a semiconductor chip carrier, comprising
4 the steps of:

5 providing a substrate, having a plated through hole therein;
6 depositing a redistribution layer on a first and a second
7 surface of the substrate; and
8 forming a via within the redistribution layer, selectively
9 positioned over and electrically contacting the plated through
10 hole.

1 16. The method of claim 15, further including the step of:
2 forming a chip connection pad in the via.

1 17. The method of claim 15, wherein the step of providing a
2 substrate, having a plated through hole therein includes the
3 steps of:

4 drilling a hole through the substrate;
5 cleaning the hole; and
6 forming a conductive layer on an interior surface of the
7 hole.

1 18. The method of claim 15, further comprising the step of:
2 filling the plated through hole with a reinforcing material.

1 19. The method of claim 18, wherein the reinforcing material
2 comprises an electrically conductive material.

1 20. The method of claim 15, wherein the step of depositing the
2 redistribution layer is performed using a lamination process.

1 21. The method of claim 15, wherein the step of providing a
2 substrate, having a plated through hole therein further includes
3 the steps of:

4 providing a ground plane;
5 forming a first pair of signal planes within the substrate;
6 forming a first pair of power cores within the substrate;
7 forming a second pair of signal planes within the substrate;
8 and
9 forming a second pair of power cores within the substrate.

1 22. The method of claim 21, wherein the first and second pair of
2 signal planes are controlled impedance circuitry.

1 23. The method of claim 21, wherein the second pair of power
2 cores are directly underneath and electrically connected to
3 portions of the redistribution layer.

1 24. The method of claim 23, wherein the second pair of power
2 cores further includes a top surface metallurgy (TSM) and a
3 bottom surface metallurgy (BSM).

1 25. The method of claim 15, wherein the redistribution layer
2 comprises a fatigue resistant dielectric material.

1 26. The method of claim 15, further comprising the step of:
2 providing a buried plated through hole in the substrate.

1 27. A semiconductor chip carrier comprising:
2 a substrate having a plated through hole therein; and
3 a/fatigue resistant redistribution layer on a first and
4 second surface of the substrate. *or directly overlying
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1 28. The semiconductor chip carrier of claim 27, further
2 comprising:

3 a via within the fatigue resistant redistribution layer,
4 positioned over and physically contacting the plated through
5 hole.

1 29. The semiconductor chip carrier of claim 27, further including
2 a buried plated through hole within the substrate.